Voltage Regulation in an Integrated Controller of a Spread-Spectrum-Clocked Buck Converter

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***Abstract*—The switching converters sometimes use spread-spectrum technique to ensure the reduction of electromagnetic emissions by distributing the energy around the clock frequency and reducing its amplitude. The change of the clock frequency naturally causes the change of the output voltage if the duty cycle is not controlled properly, i.e. kept constant. This paper presents an architecture that consists of a phase-locked loop used to generate the spread-spectrum signal and a duty cycle control circuit that ensures the constant duty cycle and consequently constant out put voltage of a buck converter. These two circuits work in close co-operation to ensure smooth transition from one clock frequency to the next in order to keep the duty cycle as constant as possible. The operation of the controller circuit is explained as well as the function of each block in the controller. The operation of the phase-locked loop is presented together with several compensation techniques used to reduce the change of the duty cycle when the clock frequency is changed. An optimal set of parameters for the exponential optimization is found.**

***Index Terms*—DC-DC converter, spread-spectrum, phase-locked loop, duty cycle compensation, on-time compensation**

I. Introduction

Increasing the switching frequency of switch-mode power DC-DC converters into a MHz range in recent years led to the appearance of the first fully integrated converters. Fully-integrated switch-mode power DC-DC converters provide several advantages over the converters designed by discrete components, such as simpler utilization, reduced cost and improved reliability [1]. One of the most important characteristics of power converters is the efficiency. Utilization of the resonant soft-switching techniques allows to reduce the switching losses and to keep the efficiency high even at the switching frequencies in the range of tens of MHz [2], [3], [4].

Increasing the switching frequency of switch-mode power DC-DC converters increases the generated electromagnetic (EM) emissions making it one of the most important challenges in the high-frequency DC-DC converter design. The maximum levels of the generated EM emissions have to be lower than the limits specified in the regulations [5]. Even a low-power devices (< 0.5 W) that are switching at the frequencies of more than 160 MHz have been reported to have failed the regulatory tests for electromagnetic compatibility (EMC) [6] [7].

Another advantage of integrated converters is the ability to use advanced management techniques at practically no cost other than the silicon area. A spread-spectrum modulator is one example of such a technique. The spread-spectrum technique is reducing the EM emissions by distributing the energy of a violating signal to the frequency band around it. Since the total energy of the signal is not changed by the modulation, the magnitudes of the spread-spectrum frequency components are reduced relative to the magnitude of the original signal.

Spread-spectrum technique is gaining popularity lately as an efficient technique for reduction of EM emission [8]. Many different switching devices already take advantage of the spread-spectrum technique, such as SATA controllers [9], audio amplifiers [10], [11] and power converters [8], [12]. Although often used in the commercial products, it was shown in [13] that many times the parameters of the spread-spectrum technique are not optimized for the given applications.

Utilization of a spread-spectrum technique is typically a trade-off – while it improves the EMC, it worsens the other characteristics of the device, e.g. the efficiency. The spread-spectrum technique which is effective for the reduction of the conducted EM emissions may not be effective for the reduction of the radiated EM emission, and vice versa. The spread-spectrum modulation in commercially available converters is usually fixed, i.e. its parameters are not user-configurable. Having a configurable spread-spectrum modulator will allow to gain the understanding of these trade-offs and enable to optimize the reduction of the generated EM emission without having to sacrifice the performance of the device (e.g. the efficiency).

The EMC measurements as described in standards CISPR 25 and IEC 61967 in the frequency range of interest (from 150 kHz to 30 MHz) use a dwell time of 200 ms [14]. Consequently, the rate, i.e. the period of frequency change used in the spread spectrum technique needs to be substantially lower. The profile of frequency change can be deterministic (e.g. sinusoidal, cubic, triangular...), but the random frequency change results in the flattest spectra as shown in [15].

This paper presents an integrated controller design used in a spread-spectrum buck converter with digitally controllable frequency and on-time. Furthermore, this paper analyses the duty cycle error caused by the spread-spectrum method and proposes an exponential on-time compensation technique.

Section II introduces the controller integrated circuit used in a spread-spectrum buck converter. The design of the controller integrated circuit is detailed in Subsection II-A which describes the analog core and Subsection II-B which describes

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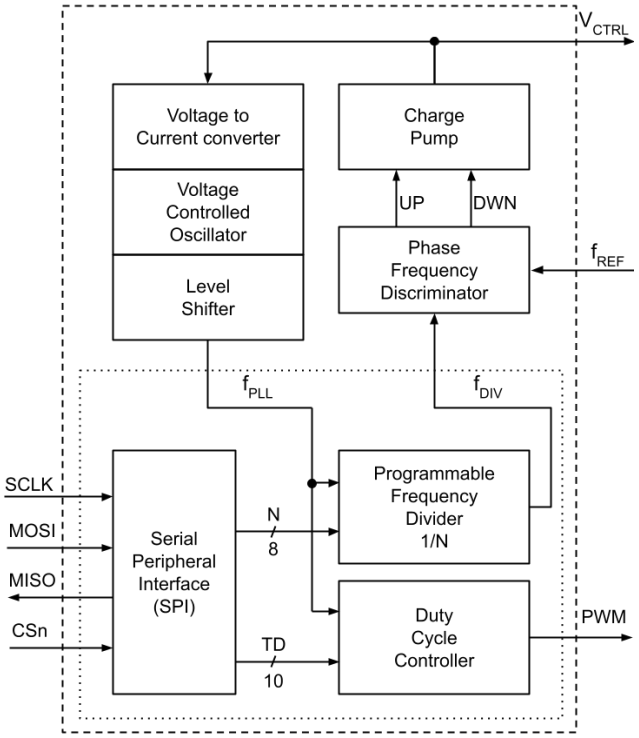

Fig. 1. The block diagram of the spread-spectrum buck converter controller.

the digital core. Section III presents the simulation results of the controller, specifically the generation of the switching frequency in the Phase Locked Loop. The output voltage regulation of a spread-spectrum buck converter is analysed in Section IV. A number of duty cycle compensation techniques are proposed in Subsection IV-A, which are then evaluated in Subsection IV-B. Section V presents the conclusions.

II. Spread-spectrum buck converter controller

Fig. 1 shows the block diagram of the spread-spectrum buck converter controller. The buck converter controller is implemented as an integrated circuit (dashed block in Fig. 1) and it consists of the analog and the digital core (dotted block in Fig. 1). The buck converter controller consists of the Phase Locked Loop (PLL), Duty Cycle Controller (DCC) and Serial Peripheral Interface (SPI). The ports of the analog core include the reference frequency signal f_{REF} and the control voltage V_{CTRL}. The ports of the digital core include the SPI communication interface signals (SCLK, MISO, MOSI and CSn) and the output Pulse Width Modulated (PWM) signal.

A. Analog core of the testchip

The analog section of the spread-spectrum buck converter controller consists of a charge-pump PLL whose architecture is described by the upper half of the block diagram in Fig. 1.

The circuit is designed for operation with a multiplication factor of 1000 to obtain the nominal output frequency f_{PLL} = 1 MHz from the input frequency f_{REF} = 1 kHz. The voltage controlled oscillator is a ring oscillator with 21 delay stages. Due to its design, a relatively high control voltage is required to obtain an output frequency of 1 MHz. If the VCO operates near its limit of the control voltage, the output voltage swing from the oscillator is reduced. During the transition to the lowest output frequency of 0.873 MHz, it is possible for the VCO to stop functioning, and in that case the output of the entire PLL would be lost. To solve this problem, an additional D flip-flop is added to the VCO output that acts as a divider by two. This means that the VCO operates at 2 MHz for a 1-MHz output frequency, but the effective value of the divider in the feedback loop is doubled. Another method of mitigating the effects of reduced output voltage swing is the addition of a level shifter on the output of the VCO.

The transfer function $H(s)$ of the PLL is described by (1). Parameter I_P is the charge pump current, while R_1, C_1, and C_2 are the components of the second-order loop filter. K_{VCO} is the gain of the VCO that represents the rate of change of the output frequency with the adjustment of the control voltage V_{CTRL}. Finally, N is the division ratio of the PLL. The damping factor ζ, natural frequency ω_n, and unity gain bandwidth ω_u (also called loop bandwidth) are described by (2)(3)(4).

$$H(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_1 N} \cdot (1 + sR_1C_1)}{s^2 + s\frac{I_P K_{VCO} R_1}{2\pi N} + \frac{I_P K_{VCO}}{2\pi C_1 N}} \tag{1}$$

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_P K_{VCO} C_1}{2\pi} \cdot \frac{1}{N}} \tag{2}$$

$$\omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_1} \cdot \frac{1}{N}} \tag{3}$$

$$\omega_u = \omega_n \cdot \sqrt{2\zeta^2 + \sqrt{4\zeta^4 + 1}} \tag{4}$$

An overview of the PLL design parameters when configured to operate with the programmable frequency divider is presented in Table I. Using the provided parameters, the calculated value of the PLL damping factor is $\zeta = 1.21$, and the loop bandwidth is $f_u = 110$ Hz. The top-level layout of the analog section of the buck converter controller is shown in Fig. 2.

The high nominal value of the division ratio N is selected because it allows for a fine adjustment of the output frequency in 1 kHz steps with the programmable frequency divider. That results in small loop bandwidth with the possibility of changing the output frequency approximately every 5 ms. The entire spread spectrum sequence can be executed in 256 steps, which would require a measurement time of 1.28 seconds for EMI conducted emissions. However, the number of spread spectrum frequencies can be lower, e.g. 128 or 64 random frequencies in a single sequence.

B. Digital core of the testchip

The Frequency Divider $1/N$ is implemented in the digital core and it is used in the feedback loop of the PLL. It divides the frequency of the output PLL signal f_{PLL} by the divider factor N. The output signal f_{DIV} is then used in the Phase

TABLE I
THE CHARGE-PUMP PLL DESIGN PARAMETERS.

Parameter	Min.	Typ.	Max.
Ref. freq. (f_{REF})		1 kHz	
Output freq. (f_{PLL})	0.873 MHz	1.000 MHz	1.128 MHz
Divider (N)	873×2	1000×2	1128×2
R_1		390 kΩ	
C_1		22 nF	
C_2		2.2 nF	
I_P		500 nA	
K_{VCO}		-7 MHz/V	

TABLE II
THE PWM AND DIVIDER PARAMETERS.

Module	Parameter	Value
Divider	Control word width	8 bits
	Nominal divider	1000
	Min. divider	873
	Max. divider	1128
PWM	Control word width	10 bits
	Max. time delay	2048 ns
	Time delay resolution	2 ns

TABLE III
THE AREA UTILIZATION OF THE DIGITAL CORE.

Cell Type	Cells []	Area [um2]	Area per. [%]
Sequential	76	3782	8.6
Combinatorial	145	2012	4.6
Delay	1025	38222	86.8
Total	1246	44016	

Frequency Discriminator to generate the PLL error signal. The divider factor N is set using a control word which is 8 bits long and the divider factor ranges from $N = 873$ to $N = 1128$ as Table II shows.

Additionally to the Frequency Divider $1/N$, the digital core consists of the Duty Cycle Controller and the Serial Peripheral Interface. The Duty Cycle Controller uses the output PLL signal f_{PLL} to define the switching signal of the buck converter. The duty cycle of the output PWM signal is determined by the on-time t_{ON} which is implemented using a variable delay line. The on-time t_{ON} is set using a control word which is 10 bits long and the on-time ranges up to $t_{ON} = 2048$ ns as Table II shows.

The design of the digital core is implemented in the TSMC 180-nm technology and Table III shows the utilization area of the digital core elaborated with respect to the cell type. Table III shows that the delay cells used in the Duty Cycle Controller take up the majority of the area (approx. 87 %).

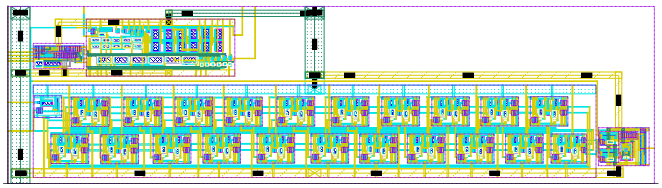

Fig. 2. The layout of the analog core (PLL).

TABLE IV
THE POWER UTILIZATION OF THE DIGITAL CORE.

Power	Value [nW]
Leakage	552
Dynamic	25696
Total	26248

The implementation results also show that the total power utilization of the digital core is approx. 26 µW. The power utilization is elaborated in Table IV which shows the leakage, dynamic and total power utilization of the digital core.

The implemented design of the digital core is shown in Fig. 3 which shows the layout of the test-chip with delay cells emphasized. The size of the implemented digital core is approx. 380x380 µm^2.

III. SIMULATIONS OF THE CONVERTER CONTROLLER

The transient response of the PLL output frequency with the change of the programmable divider value N is presented in Fig. 4. After the initial stabilization period, the divider changes from its nominal value N=1000 to its minimum value N=873 at 51 ms, and then to its maximum value N=1128 at 101 ms. Due to the presence of undershoot and overshoot, it can be concluded that $\zeta < 1$, i.e. that the actual damping factor of the PLL is smaller than the calculated value $\zeta = 1.21$ predicted by (2). The simulation result can be approximated with a step response of an ideal second-order system with $\zeta = 0.5$ and $\omega_n = 1000$ rad/s. These parameters are chosen because they provide a good fit for the frequency response and rise time in the transient characteristic. The presented transient response of the PLL is based on a pre-layout (schematic level) circuit simulation. Due to the high value of the divider N, the simulations are time-intensive and the inclusion of parasitic elements would further increase the simulation time.

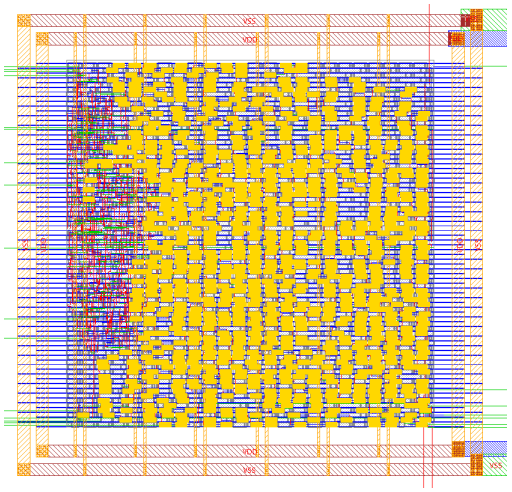

Fig. 3. The layout of the digital core of the test-chip (with delay cells emphasized).

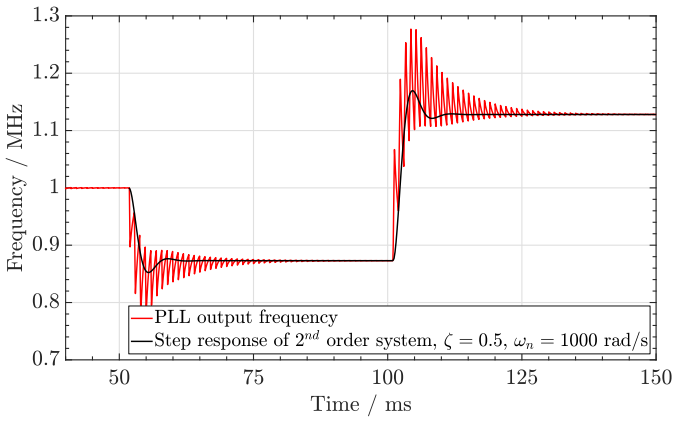

Fig. 4. Simulated response of PLL output frequency to the change of the divider value.

A smaller value of the charge pump current I_P would result in a smoother transition of the output frequency from one value to the next. This current is sourced externally and can be adjusted to improve the results. The low-pass filter components R_1, C_1, and C_2 are external to the chip and can therefore also be adjusted.

Table V presents the settling times of the value of the output frequency. The initial stabilization period is not comparable to the other results because the circuit starts from an undefined state, but it is included for reference.

Fig. 5 presents the behavior of DWN control signal on the output of the phase-frequency detector and the corresponding control voltage V_{CTRL} during the transition of the PLL division ratio from its minimum to its maximum value. While the DWN signal is active, the control voltage is reduced. Due to the negative value of K_{VCO}, the PLL output frequency is therefore increased.

IV. Voltage Regulation in a Spread-Spectrum Buck Converter

A. Compensation techniques

The buck converter uses a phase locked loop (PLL) circuit to synthesize the switching frequency of the buck converter and the switching frequency is changed by manipulating the value of the frequency divider in the feedback loop of the PLL. The change of the switching frequency is not instantaneous and both the switching frequency change and its transient affect the output duty cycle of the buck converter controller.

The output voltage V_{OUT} of a buck converter is defined as

TABLE V
PLL SETTLING TIMES.

Period	$t_{1\%}$	$t_{0.1\%}$
Initial stabilization from t=0	26.0 ms	42.0 ms
N=1000 → N=873	20.13 ms	35.17 ms
N=873 → N=1128	22.04 ms	38.02 ms

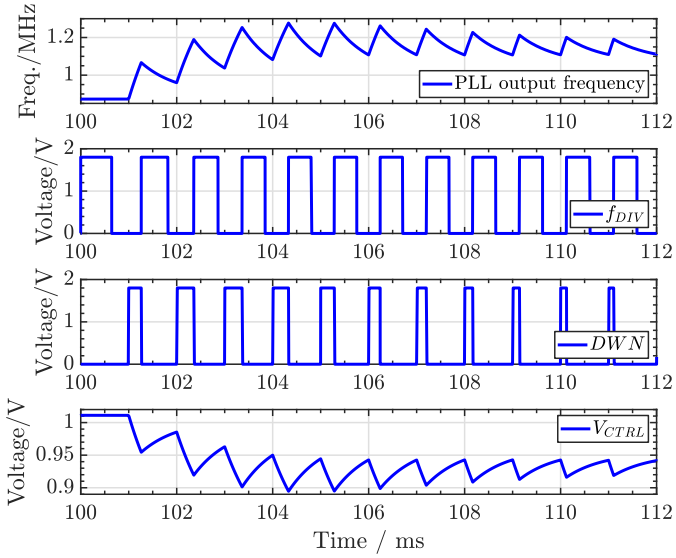

Fig. 5. The signals f_{DIV}, DWN, and V_{CTRL} during a transition of the division ratio.

$$V_{OUT} = D \cdot V_{IN} \tag{5}$$

where V_{IN} is the input voltage and D is the duty cycle of the buck converter which is defined as

$$D = \frac{T_{ON}}{T_{SW}} = T_{ON} \cdot f_{SW} \tag{6}$$

where T_{SW} and f_{SW} are the switching period and frequency of the buck converter, while T_{ON} is the on-time of the buck converter.

In a spread spectrum buck converter the switching frequency f_{SW} changes with time and consequently the on-time T_{ON} of the buck converter has to be adapted in order to preserve a constant duty cycle D and the output voltage V_{OUT}.

The basic constraint of the output voltage regulation is that the output voltage V_{OUT} remains constant regardless the changing switching frequency. The constraint is defined as

$$V_{OUT,1} = V_{OUT,2} = const. \tag{7}$$

where $V_{OUT,1}$ and $V_{OUT,2}$ are the output voltages during the time periods in which the buck converter uses switching frequencies $f_{SW,1}$ and $f_{SW,2}$, respectively. This directly translates to

$$D_1 = D_2 = D = const. \tag{8}$$

where D_1 and D_2 are the duty cycles during the time periods of the two different switching frequencies.

The reference techniques use no-compensation and simple on-time t_{ON} compensation. The no-compensation technique assumes a constant on-time t_{ON} which for nominal controller parameters is defined as

$$T_{ON} = \frac{D_{trgt}}{f_{SW,mean}} = const. \tag{9}$$

where the D_{trgt} is the desired, target value of the duty cycle of the output PWM signal of the controller.

The simple on-time compensation changes the on-time t_{ON} instantly as the divider value in the PLL divider and consequently the PLL output frequency is changed. This technique is used in the Random Carrier Frequency Modulation with Fixed Duty cycle (RCFMFD) in [17] and [18]. This compensation technique doesn't take the transient change of the output PLL frequency into account. This technique changes the on-times $T_{ON,1}$ and $T_{ON,2}$ of the buck converter during the two different switching frequencies $f_{SW,1}$ and $f_{SW,2}$ according to the relation

$$t_{ON,1} = \frac{D}{f_{SW,1}} \qquad t_{ON,2} = \frac{D}{f_{SW,2}} \tag{10}$$

This paper proposes an exponential compensation technique of the on-time τ_{ON} which uses a straightforward difference equation defined as

$$t_{ON}[n] = t_{ON}[n-1] + \frac{T_{CLK}}{\tau_C}(t_{ON,trgt} - t_{ON}[n-1]) \tag{11}$$

where $t_{ON}[n]$ and $t_{ON}[n-1]$ are the compensated on-time values at two consecutive calculation steps, T_{CLK} is the time period of the controller clock, τ_C is the time constant of the exponential compensation technique and $t_{ON,trgt}$ is the targeted, final value of the compensated on-time value which is equal to the values used in the simple compensation technique.

B. Evaluation of the compensation techniques

The reference and the proposed compensation techniques are evaluated using the simulation results shown in Fig. 4. The compensation techniques are evaluated w.r.t. the duty cycle D which is calculated using (6). To illustrate the effects of the compensation techniques the evaluation uses the part of the simulation results which represents the worst case scenario, i.e. the largest switching frequency change from minimum to maximum value. This evaluation uses an example target duty cycle $D = 35\%$.

The reference compensation techniques are calculated directly by using the on-time t_{ON} relation (9) in the case of no-compensation and relation (10) in the case of the simple compensation. Fig. 6 shows the evaluation results of the reference compensation techniques, i.e. the duty cycle without and with simple on-time t_{ON} compensation. The results show that the no-compensation case has a large duty cycle error of up to +10%. The simple compensation results show that the largest duty cycle error is at the moment the switching frequency changes and the error is approx. -7%.

The exponential compensation technique is calculated using the difference on-time t_{ON} relation (11). The sampling period is equal to the decimated simulation sampling period $T_S = 1$ µs. The exponential compensation technique is evaluated for a number of time constant values, τ_C = [0.1, 0.2, 0.5, 1.0, 2.0] ms. Fig. 7 shows the evaluation results, i.e. the duty cycle

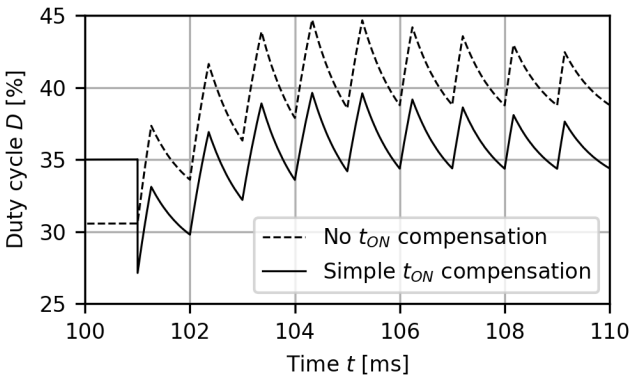

Fig. 6. The duty cycle without and with simple on-time t_{ON} compensation.

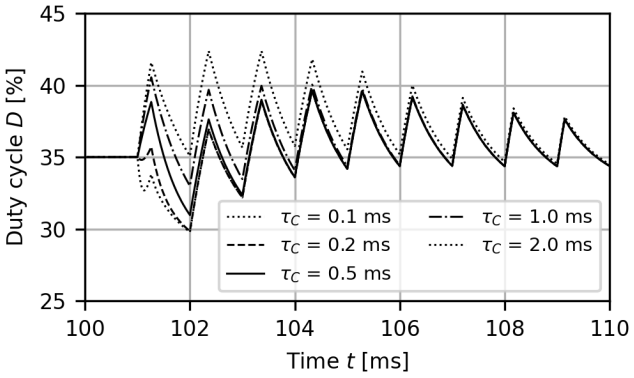

Fig. 7. The duty cycle with exponential on-time t_{ON} compensation.

with exponential on-time t_{ON} compensation. The exponential compensation results show an improvement in duty cycle error when compared to the reference compensation cases. The smallest duty cycle error is achieved in the case of the time constant $\tau_C = 0.5$ ms and it's equal to $\pm 4.64\%$.

Table VI shows the duty cycle errors of the compensation techniques. The evaluated duty cycle errors are the Root-Mean-Square (RMS) error and the Maximum Absolute Error (MAE). These results confirm the conclusion that using no-compensation causes the worst duty cycle error, while the simple compensation offers a notable improvement in duty cycle error. Further improvement in duty cycle error is achieved by using the exponential compensation technique with an optimal value of the time constant $\tau_C = 0.5$ ms.

V. Conclusions

The switching converters sometimes use spread-spectrum technique to ensure the reduction of electromagnetic emissions by distributing the energy around the clock frequency and reducing its amplitude. The change of the clock frequency naturally causes the change of the output voltage if the duty cycle is not controlled properly, i.e. kept constant. This paper presents an architecture that consists of a phase-locked loop used to generate the spread-spectrum signal and a duty

TABLE VI
THE ERRORS OF THE COMPENSATION TECHNIQUES.

Compensation	τ_C **[ms]**	**RMS [%]**	**MAE [%]**
None	N/A	5.53	9.69
Simple	N/A	2.28	7.87
	0.1	2.12	5.21
	0.2	2.05	5.16
Exponential	0.5	1.93	4.64
	1.0	2.16	5.54
	2.0	3.19	7.38

cycle control circuit that ensures the constant duty cycle and consequently constant out put voltage of a buck converter. These two circuits work in close co-operation to ensure smooth transition from one clock frequency to the next in order to keep the duty cycle as constant as possible. The phase-locked loop was simulated and the simulations show that changing the output frequency from its mean $f_{mean} = 1.000$ MHz to minimum value $f_{min} = 0.873$ MHz results in the settling time $t_{0.1\%} = 35.17$ ms, while changing the output frequency from the minimum to maximum value $f_{max} = 1.128$ MHz results in the settling time $t_{0.1\%} = 38.02$ ms. The paper analyses a number of compensation techniques used in the duty cycle controller which minimize the changes in the output duty cycle. When the duty cycle controller uses no compensation, output duty cycle has a large error of up to +10%. The simple compensation improves the duty cycle error which is in this case up to +7.87%. The exponential compensation further improves the duty cycle error and the maximum error in the case of an optimal value of the time constant $\tau_C = 0.5$ ms is equal to $\pm 4.64\%$.

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