Sizing a supercapacitor energy storage for power system applications

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***Abstract*—In this paper, we explore the issues of sizing, modelling and controlling a supercapacitor ESS (SESS) for power system applications. We give an overview of different supercapacitor models used in literature. We present a simple method for sizing a SESS taking into account a realistic supercapacitor model, calculate the energy yield and voltage profile, and give insight into supercapacitor characteristics that may cause issues if not modelled adequately.**

***Index Terms*—power system dynamics, power system simulation, power system modelling, supercapacitor, ultracapacitor, frequency control**

I. Introduction

The increasing penetration of variable renewable energy sources (RES) connected to the grid through an inverter interface brings issues of frequency stability due to the decoupling effect of inverters [1]. Thus, a lot of research effort has been given in the recent years to improve the frequency stability of power systems in the presence of high share of inverter-interfaced generation (IIG): participation of variable-speed wind turbines and solar PV plants in frequency control [2]–[5], using energy storage devices for frequency control services [6], [7], generally controlling voltage-source converter (VSC) based devices in virtual synchronous/induction generator schemes [8] and demand response.

Supercapacitors (SC), ultracapacitors (UC) or electric double-layer capacitors (EDLC) are a type of electrostatic energy storage device in which the energy is stored in the electric field between the electrodes. They are characterized by high power density and low energy density, i.e. they are good for short term power support. For grid applications, they can be used as a standalone system or in combination with batteries since their characteristics are complementary. Unlike batteries and flywheels, supercapacitors can withstand significantly more charging/discharging cycles and have smaller operation & maintenance costs since there are no moving parts and no electrochemical reactions [9]. There are many applications of supercapacitor technology, e.g. in electric vehicles [10], for power smoothing intermittent RES [11], for improving fault ride through [12] or for power system frequency control applications [6], [13]–[15].

These papers usually model the SC/UC too ideally, neglecting the voltage-dependent characteristics of a SC cell. This paper aims to discuss various characteristics of a supercapacitor and the implications of those characteristics, compare different models and give insight into sizing and controlling a SC/UC/EDLC ESS in the context of power system applications (oriented towards frequency control).

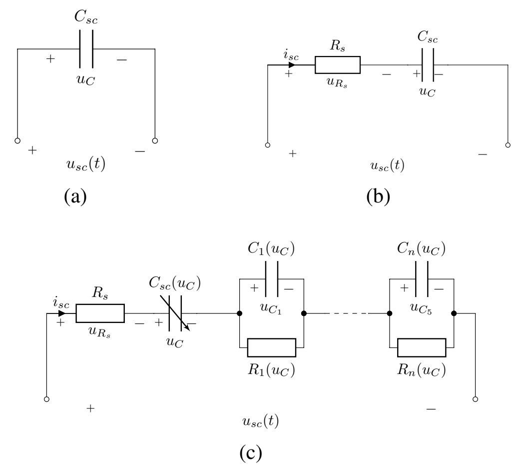

Fig. 1. Common supercapacitor models: (a) ideal model; (b) nonideal model; (c) realistic model.

II. Implications of supercapacitor modelling

In the power system applications literature, the SC is modelled either as an ideal capacitor or a constant capacitance behind an equivalent series resistance (Fig. 1(a) and Fig. 1(b), respectively). However, a realistic model of a SC obtained by experimental work [16]–[18] is shown in Fig. 1(c).

The ideal model neglects the equivalent series resistance (ESR) which will cause a voltage drop across it during charging and discharging process, and therefore the error in voltage

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measurement as well as energy dissipation. Although usually small (between 0.1 mΩ and 100 mΩ based on datasheets of commercial cells) it can have an impact on the bank efficiency especially when connecting cells in series and parallel to form a bigger supercapacitor. Note that the voltage one can measure is the total voltage including ESR, not the voltage across the actual capacitive element so the state-of-energy (SoE) must be measured in open-circuit, i.e. when the capacitor is neither charging nor discharging.

Furthermore, what both ideal and nonideal models neglect is the fact that the capacitance C_{sc} varies non-linearly with the SC voltage [16]–[18] for DC applications (the SC is not subject to periodic AC). However, for practical purposes the relationship is linear enough that it can be approximated by a linear relationship. This means that the stored energy also varies with the voltage and this might have to be considered when sizing a SC bank. Furthermore, this means that the voltage dynamics will also be different as the SC is charging or discharging.

The realistic model shown in Fig. 1(c) has been experimentally identified using procedures such as impedance spectroscopy and charge/discharge tests and validated against various real supercapacitor cells in [16]–[18]. This model only shows the first branch which describes the fast dynamic behaviour in the time scale of several tens of seconds. Parallel RC branches and leakage current branch are neglected because those phenomena are much slower (lasting from several minutes to several weeks). Although these phenomena are important when investigating the performance of the supercapacitor over tens of days, they are not important in the context of relatively fast charge/discharge for fast frequency control

The important characteristics of the realistic SC model can be summarized as follows:

- Basically all of the SC capacitance comes from C_{sc};
- Series combination of parallel branches $R_1^s C_1^s$–$R_n^s C_n^s$ is actually an infinite series of these parallel groups. However, it has been shown in [18] that five groups are sufficient to obtain an accurate model. These parallel groups model the porosity of the electrodes;
- Capacitance C_{sc} and elements R_k^s, C_k^s are dependent on $u_C(t)$. This dependence is nonlinear hence the model has the time-varying parameters. That is why an ideal capacitor representation used in many papers in the past may not always be appropriate.

Electrical parameters of the realistic model are calculated according to (1)–(4) [18].

$$C_{sc}(u_C) = C_0 + k_v u_C(t) \tag{1}$$

$$C_k^s = \frac{1}{2} C_{sc}, \quad k \in \{1...n\} \tag{2}$$

$$R_k^s = \frac{2\tau(u_C)}{k^2 \pi^2 C_{sc}} \tag{3}$$

$$\tau(u_C) \approx 3C_{sc}(R_{dc} - R_s), \tag{4}$$

C_0 is the ultracapacitor capacitance at 0 V and k_v is a constant expressed in F/V; $\tau(u_C)$ is a time constant approximated by (4); R_{dc} is the resistance experimentally obtained at very low frequencies; R_s is the equivalent series resistance (ESR) determined at very high frequency.

Voltage and current dynamics of ideal and nonideal model are described by (5), while the energy stored in steady-state ($u_C = U_{sc}$) is calculated by (6). Then, for constant discharging power (replacing i_{sc} from (5) with P/u_C and solving for u_C), voltage decay time profile (7) is obtained [6], where t is discharging time and u_{C0} is the initial SC voltage.

$$i_{sc} = C_{sc} \frac{du_C}{dt} \tag{5}$$

$$E_{id} = \frac{1}{2} C_{sc} U_{sc}^2 \tag{6}$$

$$u_C(t) = \sqrt{u_{C0}^2 - \frac{2Pt}{C_{sc}}} \tag{7}$$

However, for a realistic SC model, (5) is equal to (8) [18]. Then, the steady-state stored energy can be calculated by integrating $u_C i_{sc} d\tau$ to arrive to (9). Voltage decay profile is then given in the implicit form (10).

$$i_{sc} = (C_0 + k_v u_C) \frac{du_C}{dt} \tag{8}$$

$$E_{real} = \frac{1}{2} C_0 U_{sc}^2 + \frac{1}{3} k_v U_{sc}^3 \tag{9}$$

$$2k_v u_C^3(t) + 3C_0 u_C^2(t) = 2k_v u_{C0}^3 + 3C_0 u_{C0}^2 - 6Pt \tag{10}$$

According to literature [17], [18], the ratio of (minimum) capacitance at 0 V C_0 and (maximum) capacitance at rated voltage U_r, $\frac{C_0}{C_0 + k_v U_r}$ can range between 50% and 80%, although an example of a datasheet of modern cells [19] puts it around 80%. Based on (6) and (9), the absolute and relative errors in stored energy can be expressed by (11) and (12), respectively.

$$\Delta E = E_{id} - E_{real} = \frac{U_{sc}^2}{6} \left[3(C_{sc} - C_0) - 2k_v U_{sc} \right] \tag{11}$$

$$e_E = \frac{\Delta E}{E_{real}} \times 100\% \tag{12}$$

To calculate error in stored energy, three different voltage dependent characteristics of a realistic SC were used, differing in the magnitude of voltage dependent capacitance ($C_0/C_{max} = 0.6$—black curves, $C_0/C_{max} = 0.8$—blue curves, $C_0/C_{max} = 0.95$—red curves)—see Table I. For each SC characteristic, three ideal/nonideal models were used differing in the capacitance value: minimum ($C_{min} = C_0$), average ($C_{avg} = \frac{C_{min} + C_{max}}{2}$) and maximum ($C_{max} = C_0 + k_v U_r$). The SC module consists of ≈ 370 cells in series with rated voltage of 2.7 V each. Note that the equivalent capacitance of N_s identical cells in series can be calculated by (13).

$$C_{eqv} = \frac{C_0}{N_s} + \frac{k_v}{N_s^2} u_C(t) \tag{13}$$

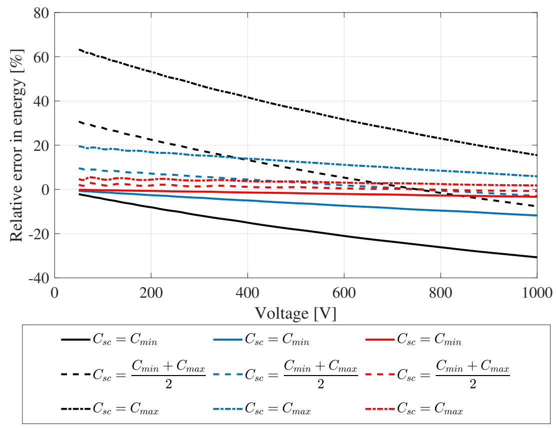

Fig. 2. Relative error in stored energy for different models

TABLE I
SUPERCAPACITOR MODELS WITH DIFFERENT VOLTAGE DEPENDENT CHARACTERISTICS USED FOR ENERGY ERROR CALCULATIONS

Model	C_0 [F]	k_v [F/V]	C_{max} [F]	U_r [V]
$\frac{C_0}{C_{max}} = 0.6$	2160	533.3	3600	2.7
$\frac{C_0}{C_{max}} = 0.8$	3000	222.2	3600	2.7
$\frac{C_0}{C_{max}} = 0.95$	3420	66.7	3600	2.7

The relative error in stored energy when ideal/nonideal model is used relative to the realistic model is shown in Fig. 2. Firstly, it can be observed that the smaller the voltage-dependent capacitance the better the ideal/nonideal models represent the SC in terms of stored energy.

For 40% voltage-dependent capacitance, the error ranges between: 15% and 60% when maximum capacitance is used, -8% and 30% when average capacitance is used and -30% and -2% when minimum capacitance is used.

For 20% voltage-dependent capacitance, the error ranges between: 6% and 20% when maximum capacitance is used, -3% and 10% when average capacitance is used and -12% and 0% when minimum capacitance is used.

For 5% voltage-dependent capacitance, the errors for all cases are inside $\pm5\%$.

Hence, one should be careful when modelling a SC with a constant capacitance models because the actual stored energy may vary significantly depending on the actual cell in question, i.e. how much the capacitance is truly constant. The issues of sizing are dealt with in the next section.

Voltage discharge profiles of a realistic, nonideal and ideal models for different discharge powers are shown in Fig. 3(a). This figure shows the 20% voltage dependent capacitance model with ideal/nonideal models with average capacitance representation. The SCs are discharged to 10% rated voltage. It can be observed that the nonideal model accurately represents the realistic model in this case, while ideal model has a slightly longer constant power discharge time (between 2% and 15% depending on the discharge power). However, these differences may be much more significant depending on the actual cell characteristics, initial voltage and discharge power. Fig. 3(b) illustrates this by showing the voltage discharge profiles (constant 0.5 MW discharge power) for a 40% variable capacitance for different ideal/nonideal representations differing in capacitance value. For the nonideal model, discharge time difference relative to the realistic model varies between -30% (minimum capacitance) and 17% (maximum capacitance). For the ideal model, this difference is between -27% (minimum capacitance) and 20% (maximum capacitance). In this case, the average capacitance was the again the most precise in terms of voltage dynamics (-7% for nonideal model, -3% for ideal model).

Notice that the nonideal and realistic models will have the voltage bounce back effect due to the ESR: the measured voltage is smaller than the actual capacitor voltage because of the voltage drop on the ESR during discharging.

The issue with constant power discharging is that the current increases as voltage decreases which will increase losses on the ESR. ESR increases when the cells are connected in series, thus when designing a SC bank for high-voltage high-power applications, a certain number of strings must be connected in parallel for two reasons:

1) to decrease the ESR;
2) to reduce the current that flows through each string.

Those two reasons will reduce the power losses and increase efficiency. Efficiency ϵ (14) curves are shown in Fig. 3(c). The higher the depth of discharge, the bigger the losses due to higher current demand. Moreover, for the same depth of discharge, higher discharge power results in bigger losses also due to higher current demand for the same voltage. Minimum achieved efficiencies are shown in Table II. They correspond to the maximum depth-of-discharge which is in this case 90%. Realistic and nonideal model have the same ESR, but the difference arises from the series combination of parallel RC groups (Fig. 1(c)). The ideal model has 100% efficiency in all cases because it has no losses as it is an ideal capacitor.

$$\epsilon(t) = \frac{u_C(t)}{u_{sc}(t)} \tag{14}$$

TABLE II
MINIMUM DISCHARGE EFFICIENCY FOR DIFFERENT MODELS

Model	Discharge power [MW]		
	0.1	1	2
Realistic	87%	45%	33%
Nonideal	90%	53%	39%
Ideal	100%	100%	100%

III. SUPERCAPACITOR BANK SIZING

In this section, it will be shown how to size a SC bank for constant power operation for frequency control services by taking into account realistic characteristics of a SC cell. The procedure is based on methodology in [20].

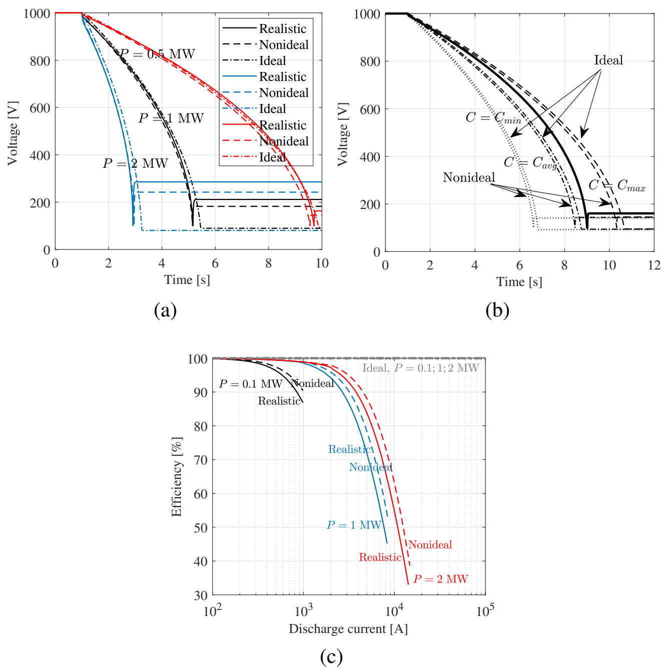

Fig. 3. Impact of modelling on supercapacitor performance: (a) voltage profile for various discharge powers; (b) voltage profile for various ideal/nonideal model capacitance values (solid black line is the realistic model); (c) discharge efficiency for various discharge powers

Although the complete voltage range of a SC (from 0V to rated) can be exploited, for constant power operation this is not possible since the current would tend towards infinity. Considering an ideal capacitor (6), 75% of energy is used between rated voltage and half the rated voltage (15).

$$\frac{E_{0.5}}{E_{max}} = \frac{\frac{1}{2}C\left(\frac{U_{max}}{2}\right)^2}{\frac{1}{2}CU_{max}^2} = \frac{1}{4} \tag{15}$$

For a realistic super capacitor, eq. (15) changes to (16).

$$\frac{E_{0.5}}{E_{max}} = \frac{1}{4}\frac{\frac{1}{2}C_0 + \frac{1}{2}\frac{k_v}{3}U_{max}}{\frac{1}{2}C_0 + \frac{k_v}{3}U_{max}} < \frac{1}{4} \tag{16}$$

This means that a realistic SC will use slightly more energy between some arbitrary voltage value and rated voltage than the equivalent ideal model. Therefore, it is not necessary to have a deep depth of discharge which increases current and losses. Approximately 84% of energy is used between $40\%U_{max}$ and U_{max}, and 91% between 30% U_{max} and U_{max}.

When sizing a storage for frequency support services, the design parameters are rated power P and duration of rated power Δt. Consider a 1 MW/30 s SESS. DC voltage range must be appropriately chosen to deliver the required power. The DC-DC converter must then be able to operate in that voltage range and be able to withstand the maximum current. For this power, an appropriate voltage range is $500-1000$ V_{dc}. The first approximation of sizing is done using a nonideal representation. First, minimum, maximum and average currents are calculated:

$$I_{min} = \frac{P}{V_{max}} = 1000 \text{ A} \tag{17}$$

$$I_{max} = \frac{P}{V_{min}} = 2000 \text{ A} \tag{18}$$

$$I_{avg} = \frac{I_{max} + I_{min}}{2} = 1500 \text{ A} \tag{19}$$

Since the ESR is unknown, in first approximation it can be estimated using a RC time constant $\tau_{RC} = RC \approx 1$ s according to commercial datasheets. Linearizing circuit equation from Fig. 1(b), total voltage change is equal to:

$$\begin{aligned}\Delta u_{sc} &= \Delta u_{R_s} + \Delta u_C \\ &= I_{avg}R_s + I_{avg}\frac{\Delta t}{C} \\ &= \frac{I_{avg}}{C}(\tau_{RC} + \Delta t)\end{aligned} \tag{20}$$

Solving for C and substituting $\Delta u_{sc} = V_{max} - V_{min}$:

$$\begin{aligned}C &= \frac{I_{avg}}{V_{max} - V_{min}}(\tau_{RC} + \Delta t) \\ &= \frac{1500}{1000 - 500}(1 + 30) = 93 \text{ F} = C_{eqv}\end{aligned} \tag{21}$$

Rated cell voltage of a SC is between 2.5 and 3 V on average. Considering a 2.7 V cell, to obtain 1000 V DC, it will require $N_s = 1000/2.7 \approx 370$ cells in series. If we have only one string ($N_p = 1$), the required cell capacitance would be $C_{cell} = C_{eqv}N_s = 34410$ F. Obviously, such a cell doesn't exist but this capacitance can be obtained by connecting cells in parallel. For $N_p = 10$, average cell capacitance is:

$$C_{cell} \approx C_{eqv}\frac{N_s}{N_p} = 93\frac{370}{10} = 3441 \text{ F} \tag{22}$$

ESR of a such a cell is around 0.29 mΩ [19] which means the equivalent ESR is:

$$R_{eqv} \approx R_s\frac{N_s}{N_p} = 0.29 \cdot 10^{-3}\frac{370}{10} \approx 10.7 \text{ m}\Omega \tag{23}$$

Since there are effectively 10 strings in parallel, each string will carry only a tenth of power, i.e. a tenth of total current therefore the losses on ESR are reduced by a factor of 100. Considering a 20% voltage-dependent capacitance, k_v and C_0 can be approximated from (24) and (25) and they are equal to 283.2 F/V and 3058.7 F, respectively.

$$C_{cell} = C_{avg} = C_0 + k_v\frac{U_{max}}{2} \tag{24}$$

$$\frac{C_0}{C_0 + k_vU_{max}} = 0.8 \tag{25}$$

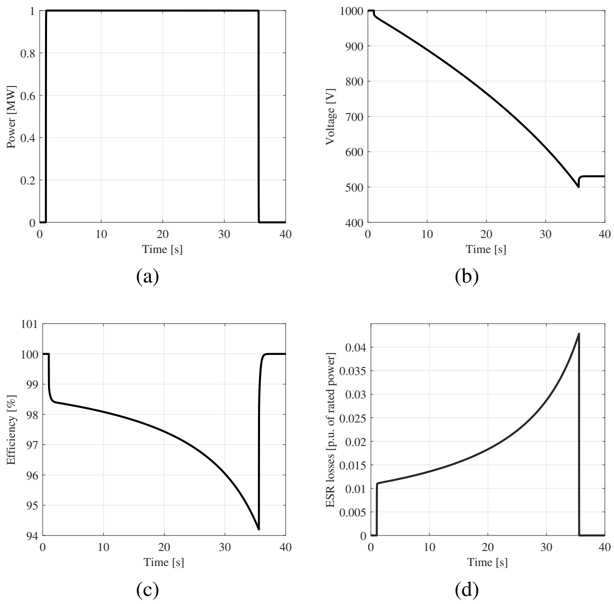

Fig. 4. Performance test of SESS design: (a) power; (b) voltage; (c) discharge efficiency; (d) ESR losses.

Now this SC bank can be simulated with a realistic model to test the performance. Results are shown in Fig. 4. This SC bank can sustain the rated power output for $\approx$ 35 seconds which is a 16% margin of error compared to requested 30 s (Fig. 4(a)). This power is discharged between the $0.5U_{max}$ and U_{max} which can be measured at the SC bank terminals (Fig. 4(b)). Discharging efficiency is between 94% and 98.5% (Fig. 4(c)), while ESR losses are between 0.01 p.u. and 0.045 p.u. (Fig. 4(d)) which is satisfactory.

The presented design procedure can be applied iteratively until satisfactory performance is achieved or if a larger margin for error is needed due to variable capacitance (e.g. 30% variable capacitance). The benefit of the presented method is that it is quite straightforward to do, even by hand, and it is based on a few simple assumptions and data that is easy to obtain from datasheets. Simulation on a realistic model then serves as a performance test for first approximation after which the process can be repeated iteratively until desired accuracy is achieved.

IV. Conclusion

In this paper, we have discussed the supercapacitor characteristics and how different modelling approaches have an impact on predicted SC performance:

- variable capacitance of the SC cell can have significant impact on the amount of energy stored and therefore on the voltage dynamics during charging/discharging;
- SC cells are very low voltage devices which need to be connected in series for high-voltage application. However, this increases losses so a balance has to be achieved with parallel strings to reduce losses;
- constant power operation can be achieved only for a limited voltage range due to current limitations—around 75% of energy can be utilized between half the rated voltage and rated voltage.

Finally, a simple iterative procedure for sizing a SESS has been presented which uses model simplifications for approximation and realistic model simulation for testing the performance.

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